CLAIMS

What is claimed is:

1. A method for supporting communication among a plurality of heterogeneous processing elements of a processing system, the method comprising:

forming an interconnection network to support services between any two processing nodes within a plurality of processing nodes;

utilizing a predefined data word format for communication among the plurality of processing nodes on the interconnection network, the predefined data word format indicating a desired service; and

arbitrating among communications in the network to ensure fair access to the network by each processing node.

2. The method of claim 1 wherein forming an interconnection network further comprises forming connections between each node in a grouping of nodes and between each of a plurality of groupings.

3. The method of claim 2 wherein the grouping of nodes further comprises a grouping of four nodes.

4. The method of claim 3 further comprising utilizing a matrix element as a processing node.

5. The method of claim 4 further comprising utilizing a RISC element as a processing node.

6. The method of claim 1 wherein forming an interconnection network further comprises forming a network of connections to support services in a point-to-point manner.

7. The method of claim1 further comprising utilizing the interconnection network to support services between a node and a host processor external to the plurality of processing nodes.

8. The method of claim 7 wherein forming an interconnection network to support services further comprises forming an interconnection network to support a host DMA service, a node DMA service, a host read/write service, and a node read/write service.

9. The method of claim 1 wherein utilizing a predefined data word format further comprises utilizing a data word format that includes a service field, a node field, a tag field, and a data field.

10. The method of claim 9 wherein the data word format further comprises a 30-bit data word.

11. The method of claim 1 wherein arbitrating further comprises transferring priority of access to the interconnection network in a round-robin manner among the plurality of processing nodes.

12. A system for supporting communication among a plurality of processing elements, the system comprising

a plurality of heterogeneous processing nodes organized as a plurality of groupings;

an interconnection network for supporting data services within and among the plurality of groupings as indicated by a data word sent from one processing node to another; and

a plurality of arbiters for directing data word traffic on the interconnection network to allow fair and efficient utilization of the interconnection network by the plurality of heterogeneous processing nodes.

13. The method of claim 12 wherein each grouping in the plurality of groupings further comprises four processing nodes.

14. The system of claim 12 wherein the plurality of arbiters provide arbitration within and among each grouping in a token-based, round robin manner.

15. The system of claim 12 further comprising a matrix as a processing node type.

16. The system of claim 12 further comprising a RISC processor as a processing node type.

17. The system of claim 12 further comprising a host processor coupled to the plurality of heterogeneous processing nodes via the interconnection network.

18. The system of claim 12 wherein the data word further comprises a plurality of bits organized as a services field, a node identification field, a tag field, and a data field.

19. The system of claim 12 wherein the communications network supports DMA services and read/write services.

20. A method for supporting communications among a plurality of processing elements, the method comprising:

organizing a plurality of heterogeneous processing nodes as separate groups of processing nodes;

providing one set of wires to support a plurality of separate processing services among and within each separate group;

communicating a data word that indicates the desired processing service from one point to another point within the plurality of heterogeneous processing nodes via the set of wires.

21. The method of claim 20 wherein each separate group further comprises four nodes.

22. The method of claim 21 wherein the four nodes further comprise three matrix elements and a RISC element.

23. The method of claim 20 further comprising arbitrating within and among the separate groups of nodes for utilization of the set of wires.